UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,881	07/15/2003	Jun Koyama	0553-0270.01	7474

7590 05/01/2006

Edward D. Manzo
Cook, Alex, McFarron, Manzo,
Cummings & Mehler, Ltd.
200 West Adams St., Ste. 2850
Chicago, IL 60606

EXAMINER	
SAID, MANSOUR M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,881	KOYAMA, JUN	
	Examiner	Art Unit	
	MANSOUR M. SAID	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,12-17,27,28,30-35 and 38-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,12-17,27,28,30-35 and 38-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/03 & 1/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1-2, 4-5, 7, 12-13, 15, 27-28, 30-31, 33, 38-39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moya et al. (6,469,405; hereinafter referred to as Moya) in view of Yamada et al. (5,990,629; hereinafter referred to as Yamda).

As to claim 1, Yamada teach a method of driving a display device which comprises a pixel comprising an EL element and a thin film transistor (figures 1, 3, 10, 12, and 16-17) and (column 5, line 40 through column line 17) comprising the step of: dividing one frame period into plural sub-frame periods (column 5, lines 40-45), and applying one of a first gate voltage and a second gate voltage to a gate electrode of the thin film transistor during each of the plural sub-frame periods (figures 1, 6 & 10-12, column 13, lines column 14, lines 28-67, column 15, lines 1-67), wherein a drain current of the thin film transistor flows between both electrodes of the EL element to place the EL element into an emitting state when the first gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 6, lines 10-67, column 14, lines 10-67, column 23, lines 40-67, and column 25, lines 45-59), wherein the thin film transistor is placed into a non-conductive state and the EL element is placed into a non-emitting

state when the second gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 15, lines 1-54, column 23, lines 40-67, and column 25, lines 60-65).

Yamada does not expressly teach wherein the thin film transistor is operated in a saturation region in order to keep said drain current constant with respect to temperature variations.

However, Moya teaches wherein the thin film transistor is operated in a saturation region in order to keep said drain current constant with respect to temperature variations (rationale same property or behavior of having a constant drain current when operating in saturation region in both TFT and FET) (figure 13, column 11, lines 31-29-32, column 18, lines 22-56, and column 19, lines 1-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Moya's teaching into Yamada's device, which is reduces the adverse affect of the switching noise on the constant current property, so as to reduce a change in the output current value due to the temperature change, which can be connected to the light emitting element panel for color display (column 4, lines 45-55).

As to claim 2, Yamada teach a method of driving a display device which comprises a pixel comprising an EL element and a thin film transistor (figures 1, 3, 10, 12, and 16-17) and (column 5, line 40 through column line 17) comprising the step of: dividing one frame period into plural sub-frame periods (column 5, lines 40-45), and applying one of a first gate voltage and a second gate voltage to a gate electrode of the thin film transistor during each of the plural sub-frame periods (figures 1, 6 & 10-12, column 13, lines column 14, lines 28-67, column 15, lines 1-67), wherein a drain current of the thin film transistor flows between both electrodes of

the EL element to place the EL element into an emitting state when the first gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 6, lines 10-67, column 14, lines 10-67, column 23, lines 40-67, and column 25, lines 45-59), wherein the thin film transistor is placed into a non-conductive state and the EL element is placed into a non-emitting state when the second gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 15, lines 1-54, column 23, lines 40-67, and column 25, lines 60-65).

Yamada does not expressly teach wherein the thin film transistor is operated in a saturation region in order to keep said drain current constant with respect to temperature variations.

However, Moya teaches wherein the thin film transistor is operated in a saturation region in order to keep said drain current constant with respect to temperature variations (rationale same property or behavior of having a constant drain current when operating in saturation region in both TFT and FET) (figure 13, column 11, lines 31-29-32, column 18, lines 22-56, and column 19, lines 1-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Moya's teaching into Yamada's device, which is reduces the adverse affect of the switching noise on the constant current property, so as to reduce a change in the output current value due to the temperature change, which can be connected to the light emitting element panel for color display (column 4, lines 45-55).

As to claims 4, 12, 30 & 38, Yamada teach wherein the EL element enables color display by using an EL layer, which emits light of one color in combination with a color conversion

layer (figures 1-13, column 13, lines 45-53, column 16, line 66 through column 17, line 14, column 22, lines 15-31, column 24, lines 35-50, and column 31, lines 18-34).

As to claims 5, 13, 31, & 39, Yamada teach wherein the EL element enables color display by using an EL layer, which emits white light, in combination with a color filter (figures 1-13, column 13, lines 45-53, column 16, line 66 through column 17, line 14, column 22, lines 15-31, column 24, lines 35-50, and column 31, lines 18-34).

As to claims 7, 15, 33 & 41, Yamada teach wherein the low molecular weight organic material is one of Alq3 (tds-8-uinolinolato-zllminllm) and TPD (triphenylnmine derivative) (column 8, lines 19-67).

As to claim 27, Yamada teach a method of driving a display device which comprises a pixel comprising an EL element and a transistor by a time gray scale method (figures 1, 3, 10, 12, and 16-17) and (column 5, line 40 through column line 17), comprising the step of: applying one of a first gate voltage and a second gate voltage to a gate electrode of the transistor (figures 1, 6 & 10-12, column 13, lines column 14, lines 28-67, column 15, lines 1-67), wherein the EL element is placed into an emitting state when the first gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 6, lines 10-67, column 14, lines 10-67, column 23, lines 40-67, and column 25, lines 45-59), wherein the EL element is placed into a non-emitting state when the second gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 15, lines 1-54, column 23, lines 40-67, and column 25, lines 60-65).

Yamada does not teach wherein the thin film transistor is operated in a saturation region when the first voltage is applied to the gate electrode of the transistor to place the EL element in the emitting state.

However, Moya teaches wherein the thin film transistor is operated in a saturation region when the first voltage is applied to the gate electrode of the transistor to place the EL element in the emitting state (rationale same property or behavior of having a constant drain current when operating in saturation region in both TFT and FET) (figure 13, column 11, lines 31-29-32, column 18, lines 22-56, and column 19, lines 1-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Moya's teaching into Yamada's device, which is reduces the adverse affect of the switching noise on the constant current property, so as to reduce a change in the output current value due to the temperature change, which can be connected to the light emitting element panel for color display (column 4, lines 45-55).

As to claim 28 Yamada teach a method of driving a display device which comprises a pixel comprising an EL element and a transistor by a time gray scale method (figures 1, 3, 10, 12, and 16-17) and (column 5, line 40 through column line 17), comprising the step of: applying one of a first gate voltage and a second gate voltage to a gate electrode of the transistor (figures 1, 6 & 10-12, column 13, lines column 14, lines 28-67, column 15, lines 1-67), wherein the EL element is placed into an emitting state when the first gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 6, lines 10-67, column 14, lines 10-67, column 23, lines 40-67, and column 25, lines 45-59), wherein the EL element is placed into a non-emitting state when the second gate voltage is applied to the gate electrode of the transistor (figures 1 & 8-11, column 15, lines 1-54, column 23, lines 40-67, and column 25, lines 60-65).

Yamada does not teach wherein the thin film transistor is operated in a saturation region when the first voltage is applied to the gate electrode of the transistor to place the EL element in the emitting state.

However, Moya teaches wherein the thin film transistor is operated in a saturation region when the first voltage is applied to the gate electrode of the transistor to place the EL element in the emitting state (rationale same property or behavior of having a constant drain current when operating in saturation region in both TFT and FET) (figure 13, column 11, lines 31-29-32, column 18, lines 22-56, and column 19, lines 1-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Moya's teaching into Yamada's device, which is reduces the adverse affect of the switching noise on the constant current property, so as to reduce a change in the output current value due to the temperature change, which can be connected to the light emitting element panel for color display (column 4, lines 45-55).

3. Claims 6, 8-9, 14, 16-17, 32, 34-35, 40, & 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Moya as applied to claims 1 & 27-28 above, and further in view of Gates et al. (6,704,133 B2; hereinafter referred to as Gates).

As to claims 6, 14, 32 & 40, Yamada and Moya teach all claimed limitation except that wherein an EL layer of the EL element comprises one of a low molecular weight organic material and a polymeric organic material.

However, Gates teaches wherein an EL layer of the EL element comprises one of a low molecular weight organic material and a polymeric organic material (column 3, lines 3-7,

column 4, lines 8-20, column 13, line 49 through column 14, line 10, and column 28, line 51 through column 29, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Gates's teaching into Yamada's modified device so that the electroluminescent display to be driven at lower brightness, thus increasing its working life (column 29, lines 1-6).

As to claims 8, 16, 34 & 42, Yamada and Moya teach all claimed limitation except that wherein the polymeric organic material is one of PPV (polyphenylene vinylene), PVK (polytvinylcarbazole), and polycarbonate.

However, Gates teaches wherein the polymeric organic material is one of PPV (polyphenylene vinylene), PVK (polytvinylcarbazole), and polycarbonate (column 3, lines 3-7, column 43-40, lines 1-19, column 6, lines 17-65, and column 28, line 51 through column 29, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Gates's teaching into Yamada's modified device so that the electroluminescent display to be driven at lower brightness, thus increasing its working life (column 29, lines 1-6).

As to claims 9, 17, 35 & 43, Yamada and Moya teach all claimed limitation except that wherein the EL layer of the EL element comprises an inorganic material.

However, Gates teaches wherein the EL layer of the EL element comprises an inorganic material (column 3, lines 3-7, column 9, lines 1-19, and column 28, line 51 through column 29, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Gates's teaching into Yamada's modified device so that the electroluminescent display to be driven at lower brightness, thus increasing its working life (column 29, lines 1-6).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MANSOUR M. SAID whose telephone number is (571) 272-7679. The examiner can normally be reached on Monday through Thursday from 8:30 a.m. to 6:00 p.m. The examiner can also be reached on alternate Friday from 8:30 a.m. to 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mansour M. Said

4/25/06

RICARDO OSORIO
PRIMARY EXAMINER